



10
↓

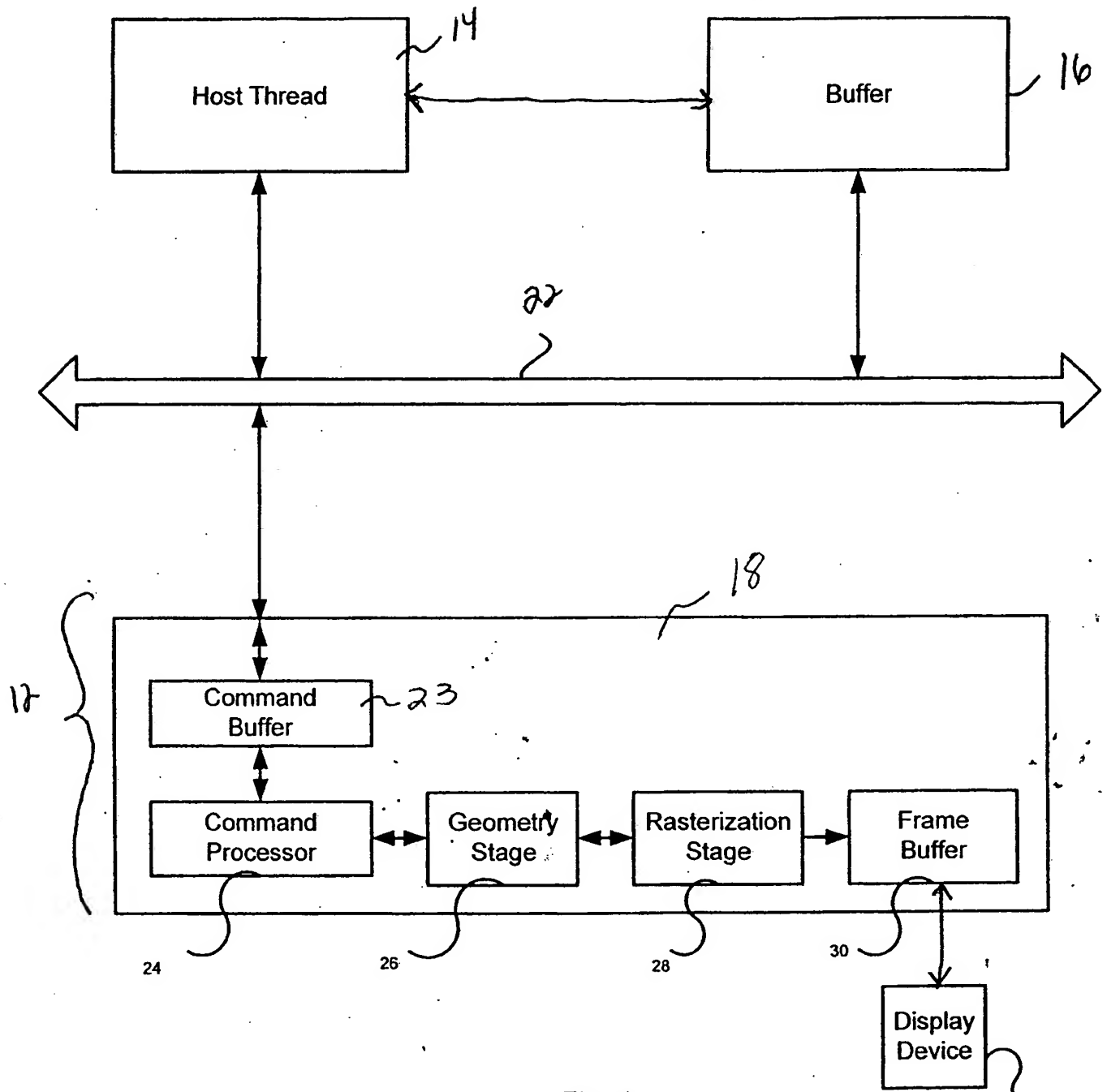


Fig. 1

20

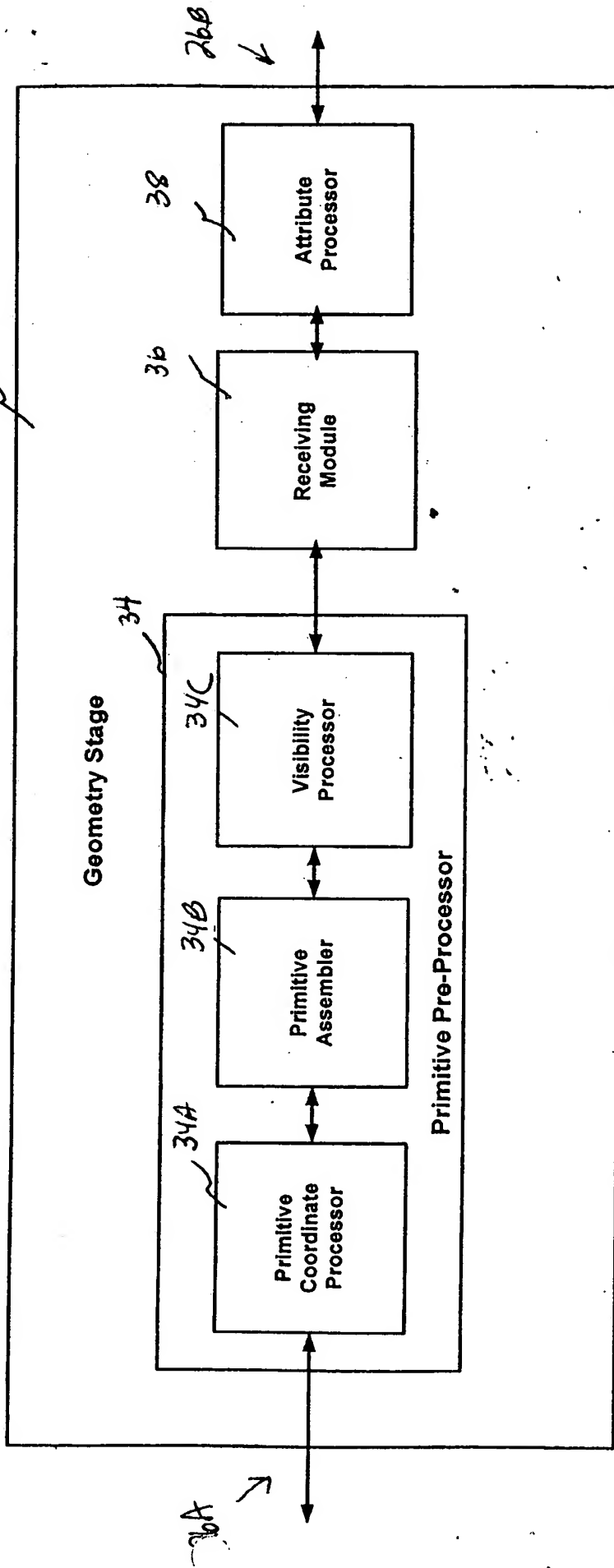


Fig. 2

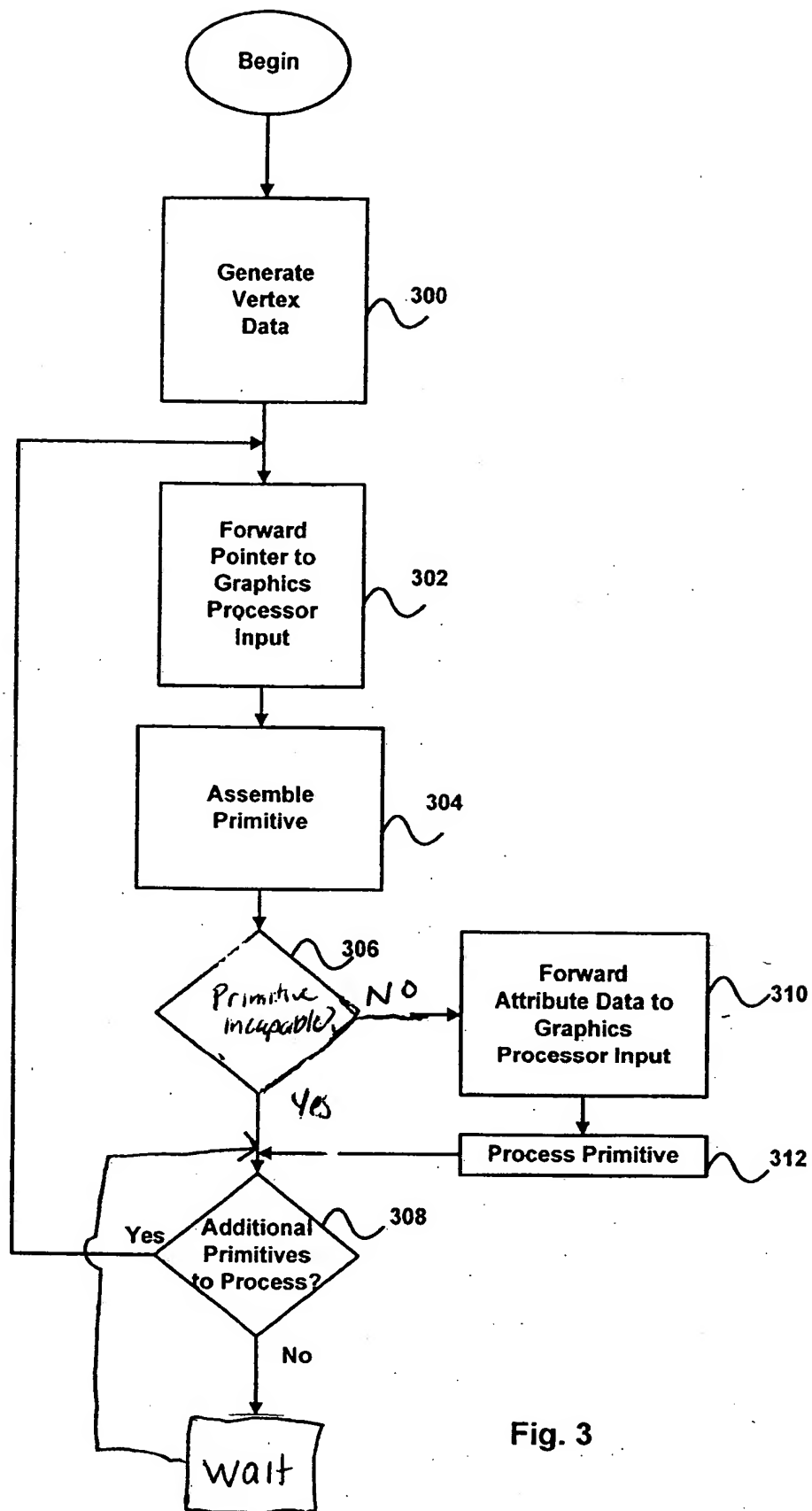


Fig. 3

16



Buffer

Address 0	Normal V1	Texture V1	Position V1
Address 1	Normal V2	Texture V2	Position V2
Address 3	Normal V3	Texture V3	Position V3
▪	▪	▪	▪
▪	▪	▪	▪
▪	▪	▪	▪
Address N-1	Normal VN	Texture VN	Position VN

Fig. 4